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(54) Photo sensor with a low-noise photo element, sub-linear response and global shutter field of the invention

(57) A photo sensor exhibiting low noise, low smear, low dark current, high dynamic range and global shutter functionality consists either of a pinned (or buried) photodiode (PPD) or a photo-sensitive charge-coupled device (CCD), each with associated transfer gate (M1), a sub-linear device (SL), a shutter transistor (M2), a reset circuit (M3) and a read-out circuit (M4,M5). Using two output paths global shutter and high speed operation are possible for the linear and the sub-linear output of the sensor. Because of its compact size, the photo sensor can be employed in one- and two-dimensional image sensors, fabricated with industry-standard CMOS and CCD technologies.

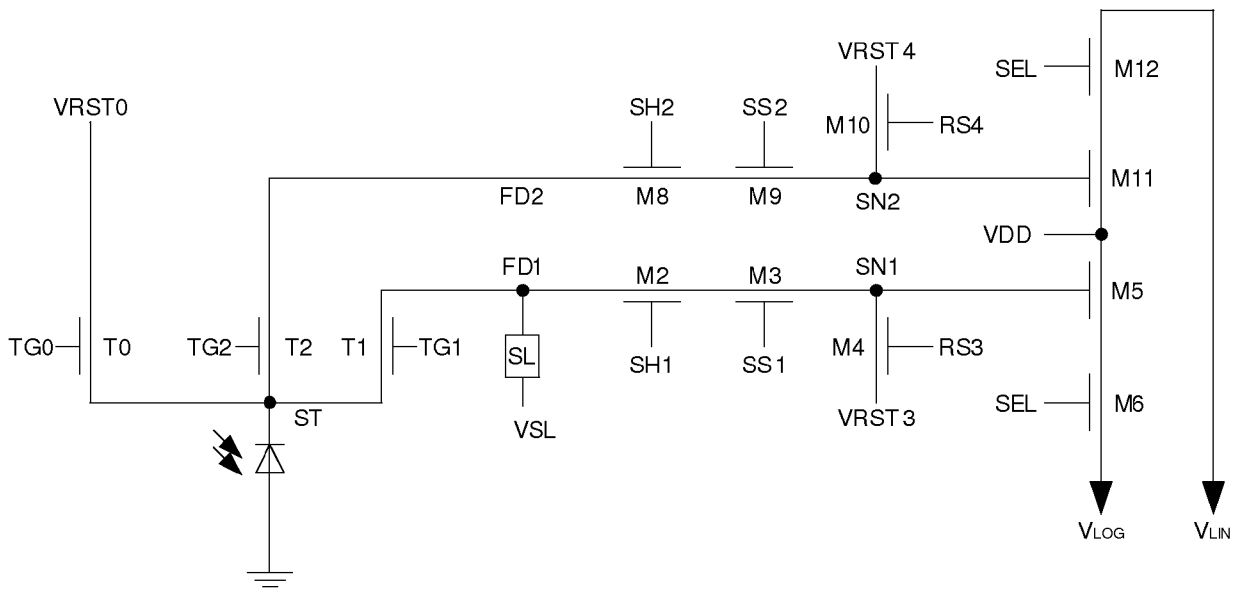

FIG. 1

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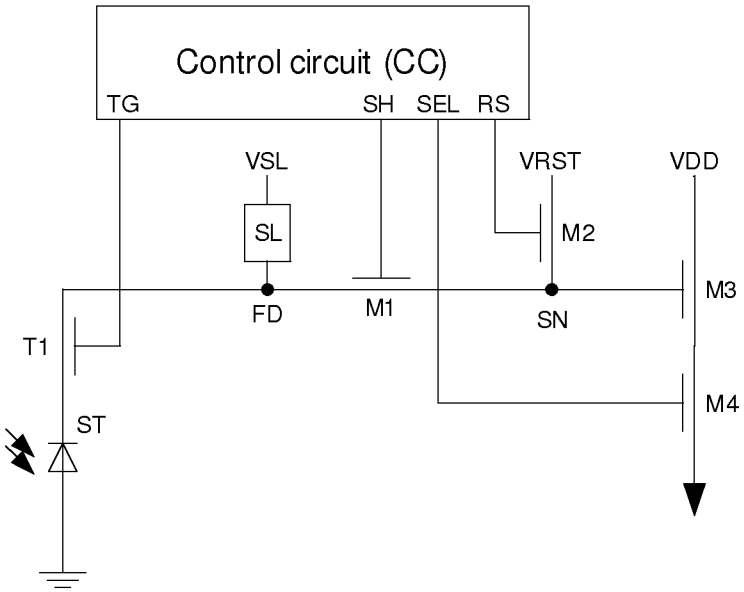

Control circuit (CC)
TG
SH
SEL
RS
VSL
VRST
VDD
SL
M2
M3
FD
M1
SN
T1
M4
ST

FIG. 7

Description

FIELD OF THE INVENTION

[0001] The present invention relates to imaging devices and more specifically, to imaging devices that are based on solid-state photo sensors.

LIST OF ABBREVIATIONS

[0002]

VSS = ground voltage
PPD = pinned photodiode
CCD = charge-coupled device
ST = pinned photodiode storage node
TG = transfer gate
VRST = reset voltage
VPIN = pinned photodiode potential
VTX = charge transfer voltage on TG
VSP = spill-over voltage on TG
VSL = sub-linear element voltage
VPRS1 = pixel reset voltage 1
VPSL = pixel's sub-linear signal voltage
VPRS2 = pixel reset voltage 2
VPLI = pixel's linear signal voltage
FD = floating diffusion
RS = reset signal for FD or SN
SH = shutter signal
SS = sampling signal
SN = sense node
SEL = pixel select signal

BACKGROUND OF THE INVENTION

[0003] Conventional photodiodes as employed in complimentary metal-oxide semiconductor (CMOS) image sensors suffer from a set of practical limitations such as elevated dark current densities that can be overcome by the use of a pinned (or buried) photodiode (PPD). Unfortunately, the advantage of the PPD regarding low dark current is obtained at the expense of a limited dynamic range of typically less than 80dB. In conventional photodiode pixels, these limitations of the dynamic range can be overcome with the use of a sub-linear device connected the cathode of the photodiode, as taught for example in US patent No. 6,815,685 (M.Wäny et al., "Photodetector and method for detecting radiation"). However this solution cannot be adopted for PPDs and charge-coupled devices (CCDs) because the storage node (ST) is internal to the device. By setting the voltage of the transfer gate (TG) to a well defined voltage to allow flowing excess charge into the floating diffusion (FD), a sub-linear element connected to **FD** generates a voltage on said node that is a sub-linear measure of the photo current.

[0004] International patent application W02007/115415 (Seitz et.al, "Photo sensor with pinned photodiode and sub-linear response") discloses a photo sensor exhibiting low noise, low smear, low dark current and high dynamic range that consists of a pinned (or buried) photodiode (PPD) with associated transfer gate (TG), a reset circuit and a device (SL) with sub-linear voltage-to-current characteristic. The storage node (Se) is external to the device.

DESCRIPTION OF THE FIGURES

[0005] The invention will be better understood and objects other than those set forth above will become apparent when consideration is given to the following detailed description thereof. Such description makes reference to the annexed drawings,
wherein:

[0006] **FIG. 1** schematically shows a pixel that allows global shutter and integrate-while-read, using two output channels for maximum speed, according to an embodiment of the invention;

[0007] **FIG. 2** schematically depicts 3 different possibilities of combining the reset transistor and the sub-linear element, according to some embodiments of the invention;

[0008] **FIG. 3** schematically shows the pixel from **FIG. 1** without a global reset at the PPD node,

[0009] **FIG. 4** schematically illustrates a modification of the pixel in FIG. 3, where only one output path is used,

[0010] **FIG. 5** schematically shows the pixel from FIG. 4 without a sampling transistor in the sub-linear path,

[0011] **FIG. 6** shows a pixel without shutter transistors, but two output paths for high speed read-out, and

[0012] **FIG. 7** schematically shows a basic pixel with sub-linear element and a shutter transistor.

[0013] **Fig. 8** shows a voltage diagram for large illumination levels.

[0014] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate identical or analog elements but may not be referenced in the description for all figures.

MODES FOR CARRYING OUT THE INVENTION

[0015] It should be noted that terms such as "first transistor", "second transistor" etc. are respectively referenced in the accompanying figures as M1, M2, etc. If e.g. M1 has a shutter function then it may also be referred to as shutter transistor M1. Abbreviated language is used in the description and in the claims.

[0016] In many solid-state imaging applications it may be desirable to employ a photo sensor having a global shutter functionality combined with low-noise and high dynamic range.

[0017] Embodiments of the present invention enable

for example the implementation of low-noise, low-smear, low-dark-current, one-dimensional and two-dimensional image sensing, where it is necessary to increase the dynamic range while having a global shutter functionality at the same time.

[0018] In particular, the invention relates in embodiments to a photo sensor for generating photoinduced charge carriers, wherein the photo sensor is implemented by one of the following: a pinned photo diode (PPD), a buried photo diode, and a charge-coupled device (CCD).

[0019] In embodiments, the photo sensor comprises at least one transfer gate to release the charge into at least one respective floating diffusion node, a sub-linear element connected to the at least one floating diffusion node, a sub-linear voltage source for which the voltage drop depends in a sub-linear fashion on a current through photo sensor, and a first transistor connected between the floating diffusion and a sense node, and a second transistor between the sense node and the reset voltage, a third transistor, a fourth transistor, a source follower and a select transistor for measuring a measured voltage indicative of a voltage at the floating diffusion node, a control circuitry adapted to run at least one measuring cycle.

[0020] In embodiments, each measuring cycle comprises the following three phases: a) in a first phase the control circuit issues a first reset command to the second transistor and toggles a shutter signal high, and transfer gate between a spill-over voltage and a charge transfer voltage to completely empty the pinned photodiode storage node of the PPD; b) in a second phase a select signal of a pixel is controlled to measure a pixel's first reset voltage, then puts the shutter signal high to measure the pixel's sub-linear signal voltage, and issues a second reset command based on the measurement, and c) in a third phase the control circuit controls the pixel select signal to measure the pixel's second reset voltage, then puts the shutter signal high and operates the transfer gate to generate the pixel's fourth linear signal voltage.

[0021] In embodiments, the first transistor M1 is a shutter transistor.

[0022] In embodiments, the photo sensor further comprises a first sub-linear reset element connected between first floating diffusion node, the sub-linear voltage source and the first reset voltage, for which a voltage drop depend in a sub-linear fashion on a current through the photo sensor, and a second sub-linear reset element connected between a second floating diffusion node, a VSS and a second reset voltage.

[0023] In embodiments, the second sub-linear reset element is a reset transistor.

[0024] In embodiments, the photo sensor further comprises a fifth transistor, wherein the second and third transistor measures a first voltage on the first floating diffusion node, and the fourth and the fifth transistor measure a second voltage on the second floating diffusion node.

[0025] In embodiments, the photo sensor further comprises a sixth, seventh and eighth transistor, wherein both the seventh and eighth transistor are operatively coupled between the second floating diffusion node and the sense node, wherein the second transistor is operatively coupled with the first floating diffusion node and the sense node, wherein the fourth transistor is operatively coupled with the reset voltage and the sense node, thus enabling the source follower and the select transistor to measure a measured the voltage at the sense node.

[0026] In embodiments, the photo sensor further comprises a ninth transistor between the second floating diffusion node, a tenth transistor, an eleventh transistor, an twelfth transistor, a first sense node, a second sense node, wherein the third transistor is operatively coupled between the first floating diffusion node and the first sense node, wherein the eighth and the ninth transistor are between the second floating diffusion node and the second sense node, wherein the fourth transistor is operatively coupled between the first sense node and a third reset voltage, wherein the tenth transistor is operatively coupled between the second sense node and a fourth reset voltage respectively, wherein the fifth and sixth transistors measure a voltage indicative of a voltage at the first sense node, and wherein an eleventh and twelfth transistor measure a voltage at the second sense node.

[0027] In embodiments, the photo sensor comprises a third transfer gate between a pinned photodiode storage node and fifth reset voltage.

[0028] In embodiments, the sub-linear element is either one of the following: a diode and a diode connected transistor.

[0029] In embodiment, the sub-linear reset element comprises either one of the following:

1 a sub-linear element and a reset transistor wherein the gate voltage has two different values, 0 and VDD; and

2 a transistor wherein the gate voltage can have three state: 0, VDD and said sub-linear voltage source.

[0030] In embodiments, the photo sensor may be implemented in CMOS-CCD hybrid image sensors whose photosensitive devices employ charge-coupled devices (CCD),

[0031] In embodiments of the invention it may be desirable to provide a photo sensor offering the advantages of a PPD or CCD combined with a sub-linear device, but also a global shutter functionality and means to enable high speed operation.

[0032] A further object of the invention is to provide methods allowing integrate-while-read, a feature that is very often used in high speed imaging.

[0033] Accordingly, in addition to the PPD or CCD phototransistor, the sensor comprises two transfer gates **(T1** and **T2)** connecting the photo active element to two nodes **FD1** and **FD2,** as is schematically illustrated in

FIG. 1. At least **FD1** comprises a sub-linear element. Both nodes have independent reset transistors associated. **FD1** is connected to node **SN1** via two transistors **(M2** and **M3)** in series. **SN1** has another reset transistor **M4** and a read-out structure **(M5** and **M6)** connected. **M6** connects to an output **VLOG.** From node **FD2** a second signal path leads to an output **VLIN.** The parallel structure from the photo-active element to outputs **VLIN** and **VLOG** enables high speed operation. The reset transistors on the nodes **FD1, FD2, SN1** and **SN2** allow integrate-while-read. The series connection of **M2** and **M3** allows storing the signal from the sensor without immediate read-out. The same holds true for **M8** and **M9.** Many photo sensors working in parallel can therefore be read-out sequentially and at the same time integrate the next signal on the photo-active element. In particular, the device can be operated in the following phases which may be part of repetitive measurement cycles:

1. Initial reset: all internal nodes are reset by activating **RS1** to **RS4.**
2. Exposure: accumulate charges on the photo-active element, set the transfer gate **(TG1)** voltage to the spill-over potential **(VSP).**
3. Global shutter for sub-linear part: **SH1** saves the sub-linear part on **FD1** to the intermediate node between **M2** and **M3**
4. Global shutter for linear part: **TG2** and **SH2** are activated to save the linear part to the intermediate node between **M8** and **M9**
5. Global reset: **FD1** and **FD2** are reset by activating **RS1** and **RS2.** The pixel is then ready for the next exposure.
6. Line by line read-out: **SEL1** and **SEL2** are activated and the column amplifiers can store the reset values of **SN1** and **SN2.** Then **SS1** and **SS2** transfer the signals to **SN1** and **SN2.** The column amplifiers can then sample the signals again and calculate the differences **VRST1-VLOG** and **VRST2-VLIN.**

[0034] The photo sensor has the potential to offer, at the same time, low noise, low image lag and smear, low dark current, a high dynamic range, a global shutter and high speed operation capabilities.

[0035] As outlined in association with the figures, it is assumed that all MOS transistors are of type NMOS. The invention however is not limit to the use of NMOS transistors. Also PMOS transistors or any combination of both types can be used to implement the pixels.

[0036] The basic operation mode is illustrated with the pixel with reference to **FIG. 7** and **FIG. 8.**

[0037] The exposure cycle is started by reverse biasing the PPD to its pinning potential and by setting the transfer gate **(TG)** to a non-zero skimming potential **(VSP).** Photo-generated charge carriers start to fill the PPD; if illumination intensity is high, excessive photo charges are flowing over the transfer gate **(T1)** to the floating diffusion node **(FD).** The sub-linear element generates a voltage on **FD** that is a sub-linear function of the illumination, hence increasing the dynamic range. The voltage at the sense node **(SN)** is read 4 times, namely at the end of the exposure time, after **M1** transferred the sub-linear voltage level from **FD** to **SN,** after reset and after the photo charge in the buried channel has been transferred via **FD** to **SN.** This allows correlated multiple sampling techniques for eliminating reset noise.

[0038] The following operation phases can be identified:

[0039] *Reset of pixel*: **FD** and **SN** are reset to **VRST** if **SH** and **RS** are both high. By pulling **TG** high as well, also the PPD is reset: the storage node is empty and settles at **VPIN.**

[0040] *Exposure*: as soon as **RS, SH** and **TG** go low, integration of photo generated charges starts: the potential on ST drops as more and more charges are accumulated up to the level VSP. Now charges spill-over into **FD.** This current generates a voltage drop over the sub-linear element.

[0041] *Read-out of sub-linear part*: the sub-linear part is read-out by activating **SEL.** The reset value **VPRS1** is available at the output of the pixel. As soon as the column amplifier sampled the value **SH** is put high to transfer the sub-linear part of the signal (if any) from **FD** to **SN** and further to the output of the pixel. The column amplifier samples **VPSL.**

[0042] *Read-out of linear part*: **RS** is again toggled low-high-low and **SH** is put low. The second reset value **VPRS2** can be stored in the column amplifier. Afterwards **SH** and **TG** go high to transfer the linear part from the **PPD** to **FD, SN** and the output of the pixel. The column amplifier can calculate the difference between **VPRS2** and **VPLI.** This scheme allows correlated double sampling of the linear part.

[0043] **FIG. 8** shows the case of large illumination levels, where the sub-linear element is activated by the charges spilling over **T1.** Consequently the linear part of the signal is equal to the full-well level of the **PPD** and does not have to be further processed.

[0044] At low illumination levels the spill-over limit is not reached and all charges are hold on **ST.** For this case the sub-linear part of the signals is zero **(FD** does not drop during the exposure time) and only a linear part exists.

[0045] Although the pixel outputs two values, only one holds the information about the illumination. Simple circuitry can be used to determine which of the two levels should be further processed in an imager implementing the pixels as described in this invention.

[0046] **FIG. 6** implements the pixel from **FIG. 7** using two read-out paths for high speed operation. **SH** is not necessary since **VPRS1** and **VPRS2** are stored on different nodes. The reset transistor and the sub-linear element are contained in the block labeled **SL/RST1** and **SL/RST2** and can be implemented using any of the three possibilities drawn in **FIG. 2:** the right most version uses the reset transistor also as the sub-linear element by con-

trolling the voltage at **RS** accordingly.

[0047] **FD1** holds the sub-linear part of the signal and **FD2** the linear part. If two SL/RST blocks are used for symmetry, the **SL** element of **SL/RST2** can be connected to the **VSS.**

[0048] **FIG. 5** shows a pixel that keeps **FD1** and **FD2** separately but uses one output path. Furthermore **SH1, SH2** and **SS** are added to implement a global shutter functionality. The column amplifier has to support two modes: **VPSL-VPRS1** and **VPRS1-VLIN** because the order at which the pixel values are output is different for the sub-linear and the linear part.

[0049] The pixel in **FIG. 4** is identical to the one of **FIG. 5** except for the fact that sampling switches are used in both paths: this allows the same processing sequence in the column amplifier, that is to say a difference between a reset voltage and a signal level.

[0050] The pixel in **FIG. 3** implements a high speed pixel with global shutter and integrate-while-read capability. In contrast to **FIG.1,** the reset of **FD1** and **FD2** are executed with **SL/RST1** and **SL/RST2** instead of **T0.** The advantage is a faster reset sequence at the expense of more complexity within the pixel.

[0051] **FIG. 1** shows a high speed, high dynamic range, low noise pixel that allows integrate-while-read operation. The sequence of operation is detailed below:

[0052] *Global reset*: **TG0** is pulled high to empty all charges from the storage node **ST** of the **PPD. RS3, RS4, SSx** and **SHx** are also high to reset all internal nodes, wherein x ε[1,2].

[0053] *Exposure:* accumulation of charges starts as soon as **TG0** is de-activated and stops when **SH1** and **TG2** were activated.

[0054] *Read-out*: the sub-linear value is sampled using **SH1.** The linear value is sampled by putting **TG2** high and toggling **SH2** as soon as **SH1** is deactivated. Now both values are stored and **TG0** can be activating to restart the next exposure immediately. **SEL** is now activated and two reset values can be sampled by the column amplifiers. Then **SS1** and **SS2** transfer the pixel values to **SN1** and **SN2** respectively where they are buffered into the column bus. As soon as the column amplifiers stored the difference to the preceding reset value the pixel is ready to be reset.

[0055] *Line reset*: **SEL** is put low, **RS3, RS4, SSx** and **SHx** are going high to reset **FDx** and **SNx** as well as the intermediate nodes of the pixel. The next line of pixels in the array can be processed.

Claims

1. A photo sensor comprising a pinned (or buried) photo diode (PPD) or a charge-coupled device (CCD) for generating photoinduced charge carriers and at least one transfer gate (T1, T2) to release said charge into a floating diffusion (FD) wherein the photo sensor further comprises
   a sub-linear element (SL) connected between the floating diffusion node (FD) and the sub-linear voltage source (VSL) for which the voltage drop depends in a sub-linear fashion on a current through the device, and a shutter transistor (M1) connected between FD and SN, and a reset transistor (M2) between SN and VRST, and transistors (M3) and (M4), a source follower and select transistor respectively for measuring a measured voltage indicative of a voltage at said node (FD), and a control circuitry adapted to run repetitive measuring cycles, wherein each measuring cycle comprises of three phases, wherein
   a) in a first phase said control circuit (CC) issues a first reset command to (M2) and toggles SH high and TG between VSP and VTX to completely empty the storage node (ST) of the PPD, and
   b) in a second phase controls SEL to measure a first voltage, VPRS1, then puts SH high to measure a second voltage, VPSL, and issues a second reset command, and
   c) in a third phase said control circuit (CC) controls SEL to measure a third voltage VPRS2, then puts SH high and operates TG to generate the fourth voltage VPLI.

2. The photo sensor of claim 1 comprising a pinned photo diode (PPD) or a charge-coupled device (CCD) for generating photo-induced charge carriers and two transfer gates (TG1 and TG2) to release said charge into floating diffusions (FD1 and FD2) **characterized in that** the photo sensor further comprises a first sub-linear reset element (SL/RST1) connected between FD1, VSL and VRST1 for which the voltage drop depend in a sub-linear fashion on a current through the device, and a second sub-linear reset element (SL/RST2) connected between FD2, VSS and VRST2.

3. The photo sensor of claim 2 where the second sub-linear reset element is replaced by a reset transistor.

4. The photo sensor of claim 2 or 3, further comprising transistors (M2) and (M3) for measuring a first voltage on FD1, and transistors (M4) and (M5) for measuring a second voltage on FD2.

5. The photo sensor of claim 2 or 3, further comprising transistor (M2) between FD1 and SN, and transistors (M7) and (M8) between FD2 and SN, and a reset transistor (M4) between VRST and SN, and transistors (M5) and (M6), a source follower and select transistor respectively for measuring a measured voltage indicative of a voltage at said node SN.

6. The photo sensor of claim 5, further comprising a

sampling transistor (M3) between M2 and SN.

7. The photo sensor of claim 2 or 3, further comprising transistors (M2) and (M3) between FD1 and SN1, and transistors (M8) and (M9) between FD2 and SN2, and reset transistors (M4) and (M10) between SN1 and VRST3 and between SN2 and VRST4 respectively, and transistors (M5) and (M6) for measuring a measured voltage indicative of a voltage at said node SN1, and transistors (M11) and (M12) for measuring a measured voltage indicative of a voltage at said node SN2.

8. The photo sensor of claim 7, further comprising a third transfer gate (TG0) between ST and VRST0.

9. The photo sensor of any of the preceding claims wherein said sub-linear element (SL) is a diode or a diode connected transistor.

10. The photo sensor of any of the preceding claims wherein said sub-linear reset element (SL/RST) comprises either a sub-linear element according to claim 8, and a reset transistor where the gate voltage has two different values, 0 and VDD, or a transistor where the gate voltage can have three state: 0, VDD and VSL.

11. The photo sensor using any of the topology of the photo sensor of any of the preceding claims consisting of NMOS- or PMOS-type of transistors.

12. The photo sensor using any of the topology of the photo sensor of any of the preceding claims using a CCD transistor as photosensitive element instead of the pinned photo diode.

13. The photo sensor array comprising a plurality of photo sensors of any of the preceding claims.

14. The camera comprising of a photo sensor array of claim 13.

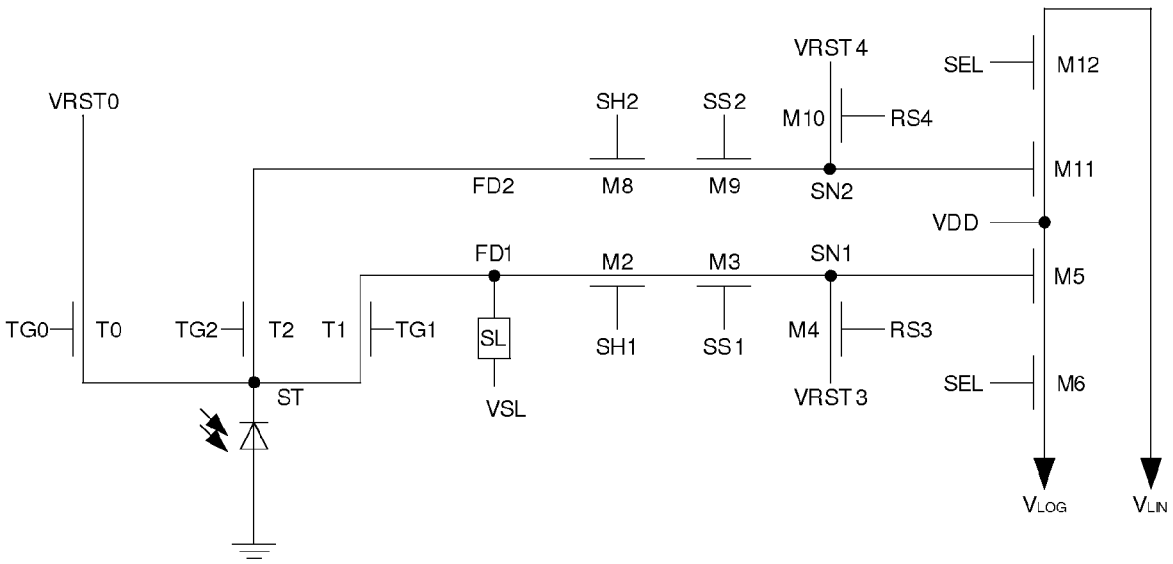

VRST0
SH2
SS2
VRST4
SEL
M12
M10
RS4
M11
FD2
M8
M9
SN2
VDD
FD1
M2
M3
SN1
M5
TG0
T0
TG2
T2
T1
TG1
SL
SH1
SS1
M4
RS3
SEL
M6
ST
VSL
VRST3
VLOG
VLIN

FIG. 1

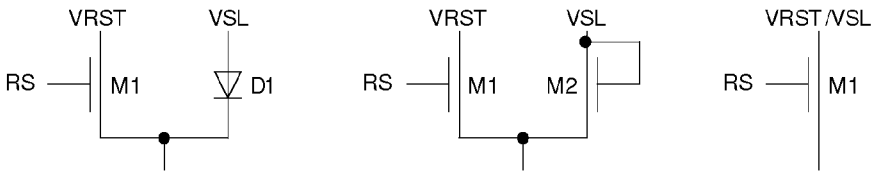

VRST
VSL
RS
M1
D1
VRST
VSL
RS
M1
M2
VRST/VSL
RS
M1

FIG. 2

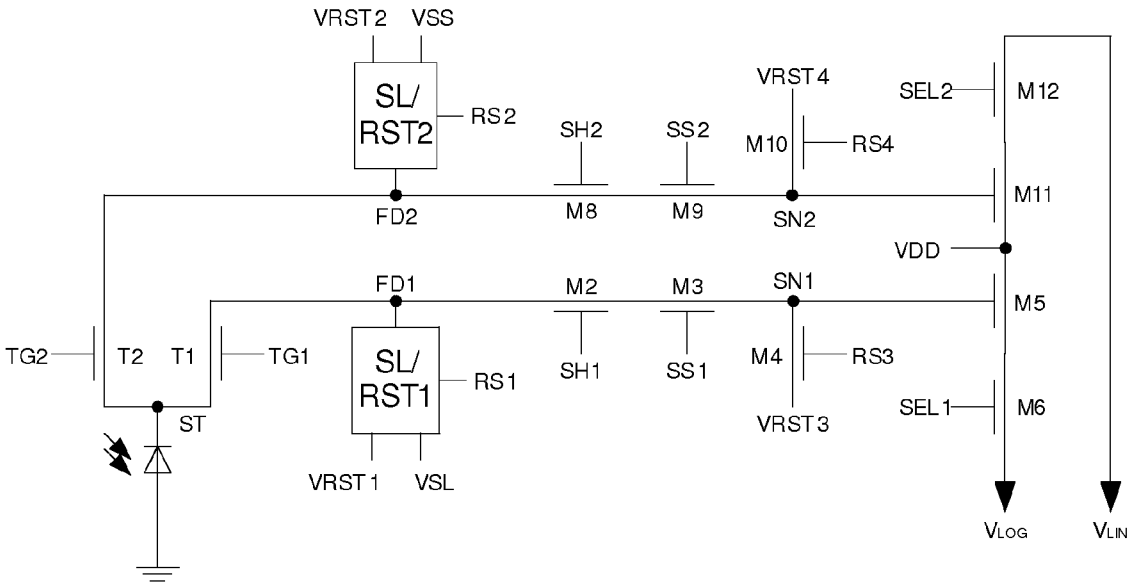

VRST2
VSS
SL/
RST2
RS2
SH2
SS2
VRST4
SEL2
M12
M10
RS4
FD2
M8
M9
SN2
M11
VDD
FD1
M2
M3
SN1
M5
TG2
T2
T1
TG1
SL/
RST1
RS1
SH1
SS1
M4
RS3
SEL1
M6
ST
VRST3
VRST1
VSL
VLOG
VLIN

FIG. 3

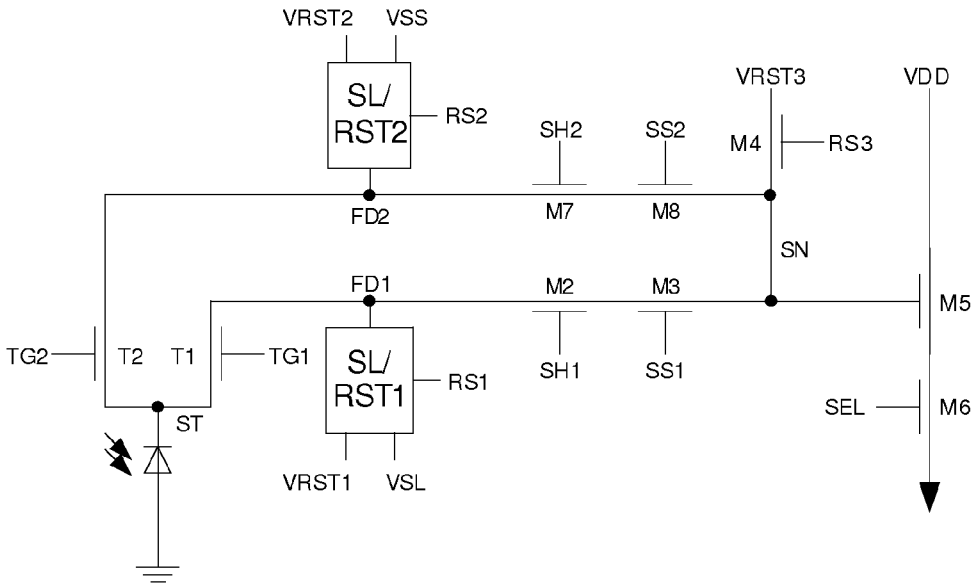
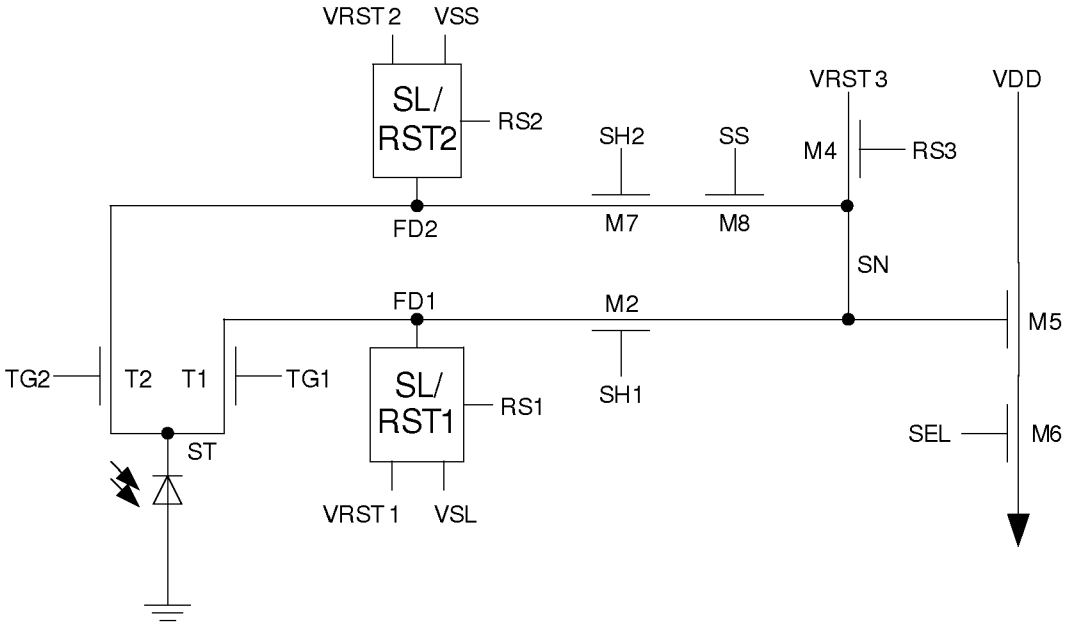

VRST2
VSS
SL/
RST2
RS2
SH2
SS2
VRST3
VDD
M4
RS3
FD2
M7
M8
SN
FD1
M2
M3
M5
TG2
T2
T1
TG1
SL/
RST1
RS1
SH1
SS1
SEL
M6
ST
VRST1
VSL

FIG. 4


VRST2
VSS
SL/
RST2
RS2
SH2
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VDD
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RS3
FD2
M7
M8
SN
FD1
M2
M5
TG2
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T1
TG1
SL/
RST1
RS1
SH1
SEL
M6
ST
VRST1
VSL

FIG. 5

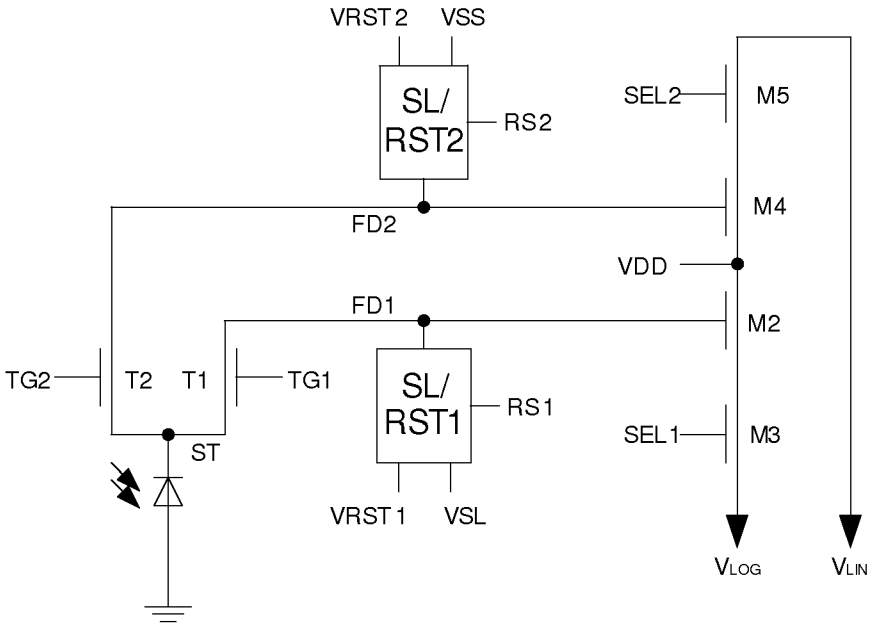
VRST2
VSS
SL/
RST2
RS2
SEL2
M5
M4
FD2
VDD
FD1
M2
TG2
T2
T1
TG1
SL/
RST1
RS1
SEL1
M3
ST
VRST1
VSL
VLOG
VLIN

FIG. 6

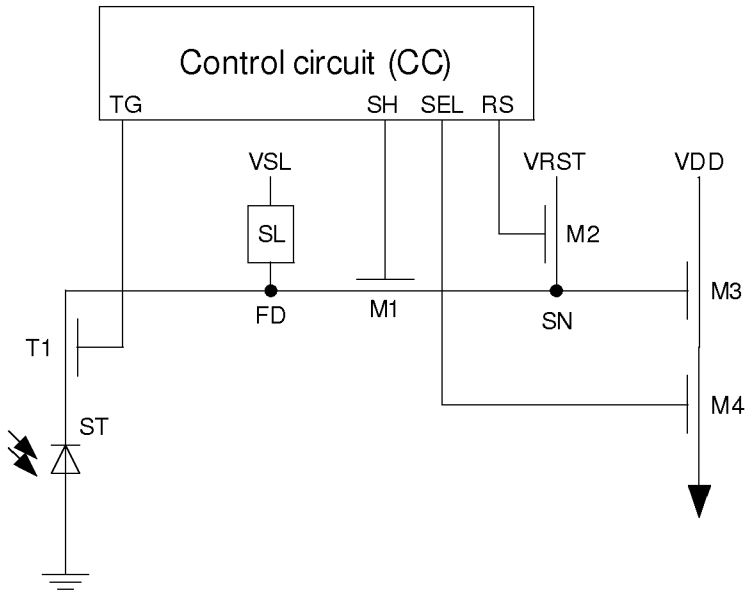
Control circuit (CC)
TG
SH
SEL
RS
VSL
VRST
VDD
SL
M2
M3
FD
M1
SN
T1
M4
ST

FIG. 7

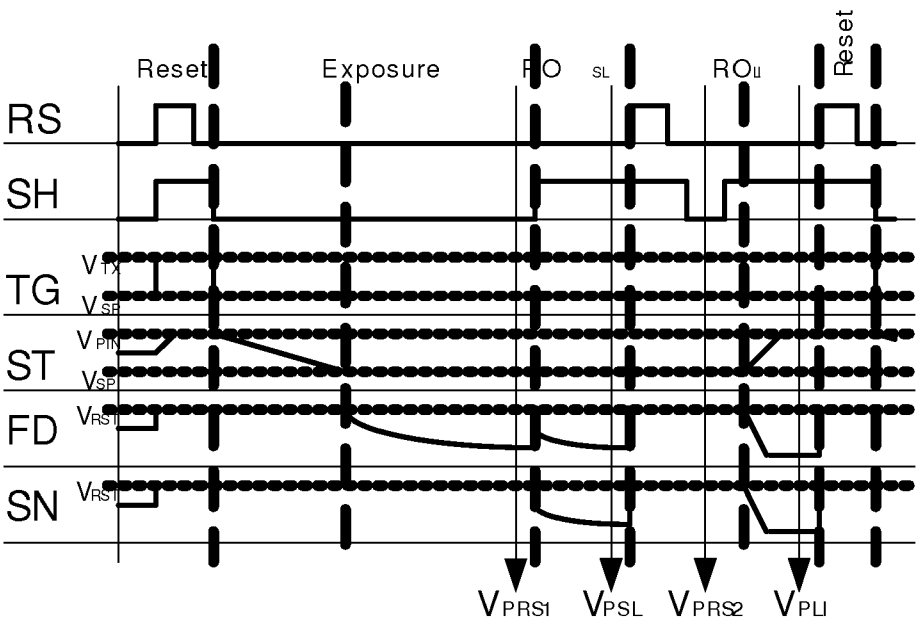
Reset
Exposure
RO SL
ROLI
Reset
RS
SH
TG
VTX
VSP
ST
VPIN
VSP
FD
VRST
SN
VRST
VPRS1
VPSL
VPRS2
VPLI

FIG. 8

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 6815685 B **[0003]**
- WO 2007115415 A **[0004]**